

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A clock delay adjusting method of a semiconductor chip integrated circuit device including hierarchical blocks, each hierarchical block including at least one clock input circuit which synchronously operates with a clock,

wherein a plurality of source points for adjusting a clock delay is provided in order to synchronize a value of the clock delay from each of the source points of each of the hierarchical blocks in a semiconductor chip to [[a]] clock input circuits, respectively, circuit to be operated synchronously with a clock depending on in accordance with [[a]] circuit design conditions ~~condition~~ of the hierarchical blocks block, and

[[an]] area terminals are terminal is provided in the source points, respectively, point, and a clock input terminal of the semiconductor chip and each area terminal are connected through a clock line so as to be clock distributed over a hierarchical top, [[and]]

a clock delay between the hierarchical blocks is adjusted, and

at least one of the hierarchical blocks has a plurality of area terminals, and wiring length to the clock input terminal from one of the plurality of area terminals is equal to that from another area terminal.

2. (Cancelled)

3. (Currently Amended) The clock delay adjusting method according to claim 1, wherein the area ~~terminal is a~~ terminals are special input terminals ~~terminal~~ for [[a]] clock input.

4. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 to 3, wherein the clock input terminal of the semiconductor chip and the area terminal are connected through a clock distribution to obtain such a wiring length as to compensate for a variation in the clock delay value of the source point in the hierarchical block.

5. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 to 3, wherein when a clock delay between the hierarchical blocks of one chip through an equal-length wiring is adjusted from the clock input terminal of the semiconductor chip to the special area terminal for a clock input of the hierarchical block and a place in which the clock delay value does not satisfy a synchronous desired value is then generated over the clock line from the special area terminal for a clock input in a certain hierarchical block to the clock input circuit, a delay adjusting buffer circuit is inserted in a place on the clock line to be an object again, thereby adjusting the clock delay and synchronizing the clock delay between the hierarchical blocks of one chip.

6. (Currently Amended) A clock delay adjusting method of a semiconductor chip ~~integrated circuit device~~ including hierarchical blocks, each hierarchical block including one or more clock input circuits which synchronously operates with a clock.

wherein an area terminal for a clock input is provided ~~in at least one place over at least one~~ to each hierarchical block ~~in a semiconductor chip~~ in accordance with a clock wiring design of the semiconductor chip,

a clock input terminal of the semiconductor chip and ~~[[the]]~~ each area terminal ~~for a clock input~~ are wired over a hierarchical top,

a difference ~~in a delay value~~ between a delay value ~~between the~~ from an area terminal ~~[[and]]~~ to the clock input terminal and a value from another area terminal to the clock input terminal is calculated, and

a clock delay ~~is adjusted~~ from the area terminal to each clock input circuit ~~circuits~~ is adjusted based on wiring length from the clock input terminal to each area terminal in order to compensate for the difference in the delay value in the hierarchical block.

7. (Original) The clock delay adjusting method according to claim 6, wherein the clock input terminal of the semiconductor chip and the area terminal for a clock input are wired over the hierarchical top in such a manner that a total clock wiring length is almost the smallest.

8. (Original) The clock delay adjusting method according to claim 6, wherein the clock input terminal of the semiconductor chip and the area terminal for a clock input are wired over the hierarchical top in such a manner that a maximum clock wiring length is almost the smallest.

9. (Original) The clock delay adjusting method according to any of claims 6 to 8, wherein a number of the clock input circuits for a clock distribution in the hierarchical block is increased from the clock input terminal of the hierarchical top to an area terminal having a small

clock delay value, and the number of the clock input circuits for a clock distribution in the hierarchical block is reduced from the clock input terminal to an area terminal having a great clock delay value, thereby adjusting a clock delay.

10. (Original) The clock delay adjusting method according to any of claims 1 or 6, wherein the clock line is formed by using a special wiring layer.

11. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 or 6, wherein the clock input terminal is constituted by a plurality of clock input terminals, and forms a multisystem clock having such a structure that a clock input is carried out from the clock input terminals to one hierarchical block.

12. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 or 6, wherein a repeater buffer circuit is further inserted in or between the hierarchical blocks on a wiring of the clock line over the hierarchical top, thereby suppressing waveform rounding of a clock signal.

13. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 or 6, wherein a plurality of clock input circuits is provided in the hierarchical block, and

the value of the clock delay of the clock line between a clock control circuit in the hierarchical block and each of the clock input circuits is adjusted by using a delay adjusting

buffer circuit when the clock control circuit is to be inserted into the clock line to each of the clock input circuits.

14. (Original) The clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 or 6, wherein a position of arrangement of the area terminal is adjusted in such a manner that a wiring path for the clock line obtained before a floor plan correction can also be reused after the floor plan correction.

15. (Original) A semiconductor integrated circuit device using the clock delay adjusting method of a semiconductor integrated circuit device according to any of claims 1 or 6.

16. (Original) The semiconductor integrated circuit device according to claim 15, wherein at least one of the hierarchical blocks includes a plurality of special area terminals for a clock input, and a clock line is constituted by a special wiring layer for the clock line which is provided as an upper layer on the area terminal.